ABSTRACT OF THE DISCLOSURE

A duty cycle correction (DCC) circuit receives first and second clock signals and outputs a duty cycle adjusted clock signal, and a control circuit detects a process variation and controls respective slew rates of the first and second clock signals based on the detected process variation. The DCC circuit may include a first inverter having an input that receives the first clock signal, a second inverter having an input that receives the second clock signal, a third inverter having an input commonly connected to outputs of the first and second inverters, a first variable capacitor connected between the input of the first inverter and a ground voltage, and a second variable capacitor connected between the input of the first inverter and the ground voltage. In this case, the respective capacitance values of the first and second variable capacitors are set by the control circuit.